# 2 K × 8 CMOS Dual Port RAM 3.3 Volt

## Introduction

The L67132/67142 are very low power CMOS dual port static RAMs organized as 2048 × 8. They are designed to be used as a stand-alone 8 bit dual port RAM or as a combination MASTER/SLAVE dual port for 16 bits or more width systems. The MHS MASTER/SLAVE dual port approach in memory system applications results in full speed, error free operation without the need for additional discrete logic.

Master and slave devices provide two independent ports with separate control, address and I/O pins that permit independent, asynchronous access for reads and writes to any location in the memory. An automatic power down feature controlled by $\overline{CS}$ permits the onchip circuitry of each port in order to enter a very low stand by power mode.

Using an array of eight transistors (8T) memory cell and fabricated with the state of the art 1.0 µm lithography named SCMOS, the L67132/67142 combine an extremely low standby supply current (typ = 1.0 µA) with a fast access time at 45 ns over the full temperature range. All versions offer battery backup data retention capability with a typical power consumption at less than 5 µW.

For military/space applications that demand superior levels of performance and reliability the L67132/67142 is processed according to the methods of the latest revision of the MIL STD 883 (class B or S) and/or ESA SCC 9000.

## Features

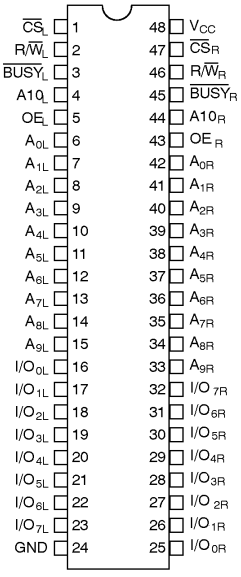
- Single 3.3 V ± 0.3 volt power supply
- Fast access time
  45(*) ns to 70 ns
- 67132L/67142L low power
  67132V/67142V very low power
- Expandable data bus to 16 bits or more using master/slave devices when using more than one device
- On chip arbitration logic
- $\overline{BUSY}$ output flag on master
- $\overline{BUSY}$ input flag on slave
- Fully asynchronous operation from either port
- Battery backup operation :
  2 V data retention

(*) Preliminary

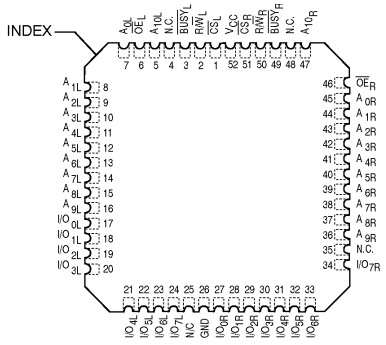
# Interface

## Pin Configuration

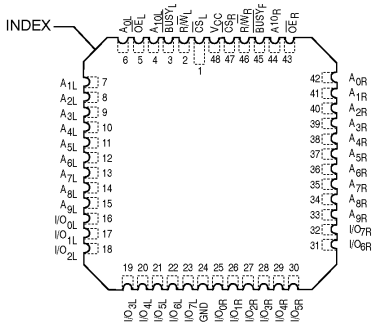
**48 PIN DIL (top view), plastic, ceramic 600 mils**



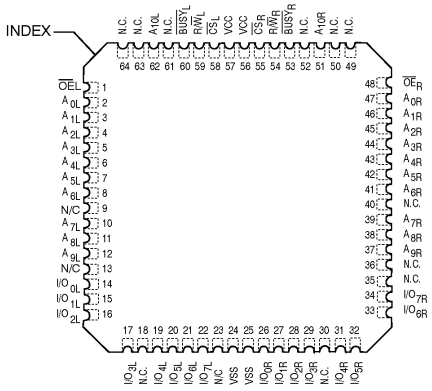

**52 PIN PLCC (top view)**



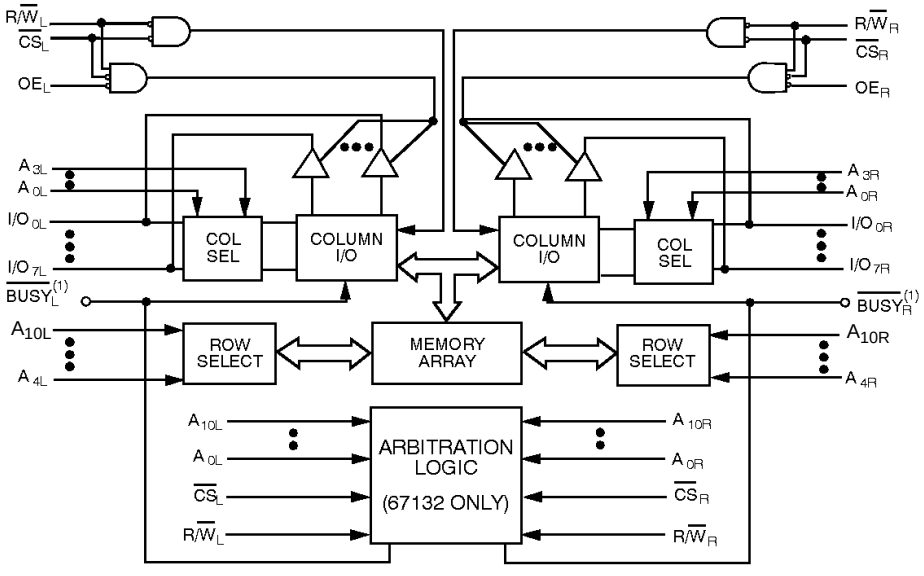

**48 PIN LCC (top view)**




**64 PIN VQFP (top view)**




## Block Diagram




**Note :** 1. L 67132 (MASTER) : $\overline{BUSY}$ is open drain output and requires pullup resistor
L 67142 (SLAVE) : $\overline{BUSY}$ in input

### Pin Names

| LEFT PORT | RIGHT PORT | NAMES |
|---|---|---|
| $\overline{CS}_L$ | $\overline{CS}_R$ | Chip select |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L-10L}$ | $A_{0R-10R}$ | Address |
| $I/O_{0L-7L}$ | $I/O_{0R-7R}$ | Data Input/Output |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag |
| VCC | | Power |
| GND | | Ground |

## Functional Description

The L67132/67142 has two ports with separate control, address and I/0 pins that permit independent read/write access to any memory location. These devices have an automatic power-down feature controlled by $\overline{CS}$. $\overline{CS}$ controls on-chip power-down circuitry which causes the port concerned to go into stand-by mode when not selected ($\overline{CS}$ high). When a port is selected access to the full memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In read mode, the port's $\overline{OE}$ turns the Output drivers on when set LOW. Non-conflicting READ/WRITE conditions are illustrated in table 1.

### Arbitration Logic

The arbitration logic will resolve an address match or a chip select match down to a minimum of 5 ns and determine which port has access. In all cases, an active $\overline{BUSY}$ flag will be set for the inhibited port.

The $\overline{BUSY}$ flags are required when both ports attempt to access the same location simultaneously.Should this conflict arise, on-chip arbitration logic will determine which port has access and set the $\overline{BUSY}$ flag for the inhibited port. $\overline{BUSY}$ is set at speeds that allow the processor to hold the operation with its associated address and data. It should be noted that the operation is invalid for the port for which $\overline{BUSY}$ is set LOW. The inhibited port will be given access when $\overline{BUSY}$ goes inactive.

A conflict will occur when both left and right ports are active and the two addresses coincide. The on-chip arbitration determines access in these circumstances. Two modes of arbitration are provided : (1) if the addresses match and are valid before $\overline{CS}$ on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for access ; or (2) if the $\overline{CS}$ are low before an address match, on-chip control logic arbitrates between the left and right addresses for access (refer to table 2). The inhibited port's $\overline{BUSY}$ flag is set and will reset when the port granted access completes its operation in both arbitration modes.

### Data Bus Width Expansion

#### Master/Slave Description

Expanding the data bus width to 16 or more bits in a dual-port RAM system means that several chips may be active simultaneously. If every chip has a hardware arbitrator, and the addresses for each chip arrive at the same time one chip may activate its L $\overline{BUSY}$ signal while another activates its R $\overline{BUSY}$ signal. Both sides are now busy and the CPUs will wait indefinitely for their port to become free.

To overcome this "Busy Lock-Out" problem, MHS has developed a MASTER/SLAVE system which uses a single hardware arbitrator located on the MASTER. The SLAVE has $\overline{BUSY}$ inputs which allow direct interface to the MASTER with no external components, giving a speed advantage over other systems.

When dual-port RAMs are expanded in width, the SLAVE RAMs must be prevented from writing until the $\overline{BUSY}$ input has been settled. Otherwise, the SLAVE chip may begin a write cycle during a conflict situation. On the opposite, the write pulse must extend a hold time beyond $\overline{BUSY}$ to ensure that a write cycle occurs once the conflict is resolved. This timing is inherent in all dual-port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE must be inhibited by the MASTER's maximum arbitration time. If a conflict then occurs, the write to the SLAVE will be inhibited because of the MASTER's $\overline{BUSY}$ signal.

## Truth Table

### Table 1 : Non Contention Read/Write Control(4)

| LEFT OR RIGHT PORT(1) | | | | FUNCTION |
|---|---|---|---|---|
| R/$\overline{W}$ | $\overline{CS}$ | $\overline{OE}$ | D0–7 | |
| X | H | X | Z | Port Disabled and in Power Down Mode. ICCSB or ICCSB1 |
| L | L | X | $DATA_{IN}$ | Data on Port Written into memory(2) |
| H | L | L | $DATA_{OUT}$ | Data in Memory Output on Port(3) |
| H | L | H | Z | High Impedance Outputs |

**Notes :** 1. $A_{OL} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see $t_{WDD}$ and $t_{DDD}$ timing.
4. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE.

### Table 2 : Arbitration(5)

| LEFT PORT | | RIGHT PORT | | FLAGS | | FUNCTION |
|---|---|---|---|---|---|---|
| $\overline{CS}_L$ | $A_{0L} - A_{10L}$ | $\overline{CS}_R$ | $A_{0L} - A_{10R}$ | $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | |
| H | X | H | X | H | H | No Contention |
| L | Any | H | X | H | H | No Contention |
| H | X | L | Any | H | H | No Contention |
| L | $\neq A_{0R} - A_{10R}$ | L | $\neq A_{0L} - A_{10L}$ | H | H | No Contention |
| **ADDRESS ARBITRATION WITH $\overline{CE}$ LOW BEFORE ADDRESS MATCH** | | | | | | |
| L | LV5R | L | LV5R | H | L | L–Port Wins |
| L | RV5L | L | RV5L | L | H | R–Port Wins |
| L | Same | L | Same | H | L | Arbitration Resolved |
| L | Same | L | Same | L | H | Arbitration Resolved |
| **$\overline{CS}$ ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$** | | | | | | |
| LL5R | $= A_{0R} - A_{10R}$ | LL5R | $= A_{0L} - A_{10L}$ | H | L | L–Port Wins |
| RL5L | $= A_{0R} - A_{10R}$ | RL5L | $= A_{0L} - A_{10L}$ | L | H | R–Port Wins |
| LW5R | $= A_{0R} - A_{10R}$ | LW5R | $= A_{0L} - A_{10L}$ | H | L | Arbitration Resolved |
| LW5R | $= A_{0R} - A_{10R}$ | LW5R | $= A_{0L} - A_{10L}$ | L | H | Arbitration Resolved |

**Notes :** 5. X = DON'T CARE, L = LOW, H = HIGH.
LV5R = Left Address Valid ≥ 5 ns before right address.
RV5L = Right address Valid ≥ 5 ns before left address.
Same = Left and Right Addresses match within 5 ns of each other.
LL5R = Left $\overline{CS}$ = LOW ≥ 5 ns before Right $\overline{CS}$.
RL5L = Right $\overline{CS}$ = LOW ≥ 5 ns before left $\overline{CS}$.
LW5R = Left and Right $\overline{CS}$ = LOW within 5 ns of each other.

# Electrical Characteristics

## Absolute Maximum Ratings

Supply voltage (VCC–GND) : . . . . . –0.3 V to 7.0 V
Input or output voltage applied : . . . (GND –0.3 V) to (VCC + 0.3 V)
Storage temperature : . . . . . –65°C to + 150°C

**** Notice***

*Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extented periods may affect reliability.*

| OPERATING RANGE | OPERATING SUPPLY VOLTAGE | OPERATING TEMPERATURE |
|---|---|---|
| Military | $V_{CC}$ = 3.3 V ± 0.3 V | – 55 °C to + 125 °C |
| Automotive | $V_{CC}$ = 3.3 V ± 0.3 V | – 40 °C to + 125 °C |
| Commercial | $V_{CC}$ = 3.3 V ± 0.3 V | 0 °C to + 70 °C |
| Industrial | $V_{CC}$ = 3.3 V ± 0.3 V | – 40 °C to + 85 °C |

## DC Parameters

| Parameter | Description | Version | L67132/67142–45 | | L67132/67142–55 | | L67132/67142–70 | | Unit | Value |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | COM | IND MIL AUTO | COM | IND MIL AUTO | COM | IND MIL AUTO | | |
| | | | PRELIMINARY | | | | | | | |
| $I_{CCSB}$ (6) | Standby supply current (Both ports TTL level inputs) | V<br>L | 1<br>5 | 1<br>10 | 1<br>5 | 1<br>10 | 1<br>5 | 1<br>10 | mA<br>mA | Max<br>Max |
| $I_{CCSB1}$ (7) | Standby supply current (Both ports CMOS level inputs) | V<br>L | 10<br>100 | 20<br>200 | 10<br>100 | 20<br>200 | 10<br>100 | 20<br>200 | µA<br>µA | Max<br>Max |
| $I_{CCOP}$ (8) | Operating supply current (Both ports active) | V<br>L | 80<br>80 | 90<br>100 | 70<br>70 | 80<br>90 | 60<br>60 | 70<br>80 | mA<br>mA | Max<br>Max |
| $I_{CCOP1}$ (9) | Operating supply current (One port active – One port standby) | V<br>L | 50<br>60 | 55<br>65 | 40<br>50 | 45<br>55 | 35<br>45 | 40<br>50 | mA<br>mA | Max<br>Max |

**Notes :** 6. $\overline{CS}_L = \overline{CS}_R \geq 2.2$ V.
7. $\overline{CS}_L = \overline{CS}_R \geq$ VCC – 0.2 V.
8. Both ports active – Maximum frequency – Outputs open – $\overline{OE}$ = VIH.
9. One port active (f = MAX) – Output open – One port stand-by TTL or CMOS Level inputs – $\overline{CS}_L = \overline{CS}_R \geq 2.2$ V.

| PARAMETER | DESCRIPTION | L67132–45/55/70<br>L67142–45/55/70 | UNIT | VALUE |
|---|---|---|---|---|
| $II/O_{(10)}$ | Input/Output leakage current | ± 10 | µA | Max |
| $VIL_{(11)}$ | Input low voltage | 0.7 | V | Max |
| $VIH_{(11)}$ | Input high voltage | 1.8 | V | Min |
| $VOL_{(12)}$ | Output low voltage ($I/O_0$–$I/O_7$) | 0.5 | V | Max |
| $VOL_{(13)}$ | Open drain output low voltage (BUSY) | 0.5 | V | Max |
| $VOH_{(12)}$ | Output high voltage | 1.5 | V | Min |
| $C\ IN_{(17)}$ | Input capacitance | 5 | pF | Max |
| $C\ OUT_{(17)}$ | Output capacitance | 7 | pF | Max |

**Notes :** 10. $V_{CC}$ = 5 V, Vin = Gnd to $V_{CC}$, $\overline{CS}$ = VIH, Vout = 0 to $V_{CC}$.
11. VIH max = $V_{CC}$ + 0.3 V, VIL min – 0.3 V or –1 V pulse width 50 ns.
12. $V_{CC}$ min, IOL = 4 mA, IOH = –4 mA.
13. $I_{OL}$ = 16 mA.

## Data-Retention Mode

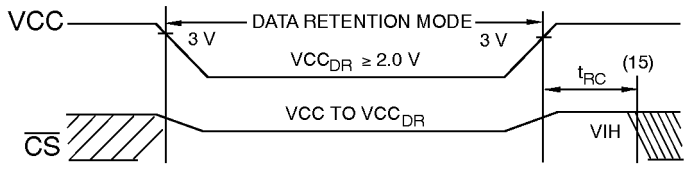
MHS CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1 – Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to $VCC_{DR}$.

2 – $\overline{CS}$ must be kept between $V_{CC}$ – 0.2 V and 70 % of Vcc during the power up and power down transitions.

3 – The RAM can begin operation > tRC after Vcc reaches the minimum operating voltage (3 volts).

## Timing




| PARAMETER | TEST CONDITIONS (14) | MAX | | UNIT |
|---|---|---|---|---|
| | | COM | MIL IND AUTO | |
| $ICC_{DR1}$ | @ $VCC_{DR}$ = 2 V | 10 | 20 | µA |

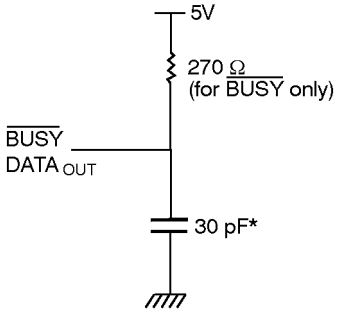
**Notes :** 14. $\overline{CS}$ = Vcc, Vin = Gnd to Vcc.

## AC Test Conditions

Input Pulse Levels : GND to 3.0 V
Input Rise/Fall Times : 5 ns
Input Timing Reference Levels : 1.5 V

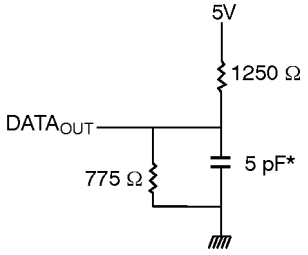
Output Reference Levels : 1.5 V
Output Load : see figures 1, 2

**Figure 1. Output Load.**




* Including scope and jig

**Figure 2. Output load.**
**(For $t_{HZ}$, $t_{LZ}$, $t_{WZ}$, and $t_{OW}$)**

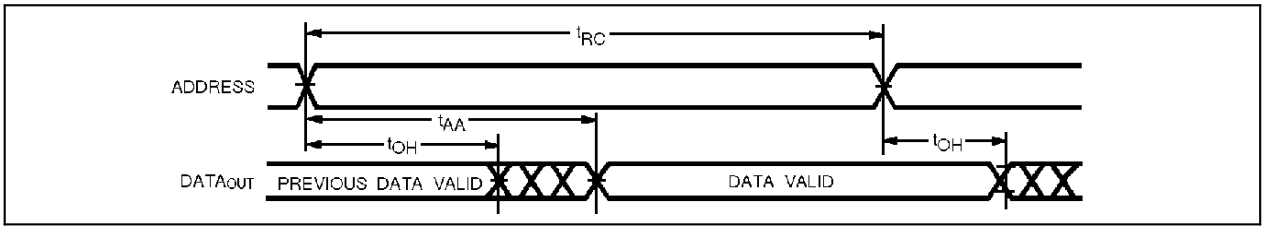


## AC Parameters

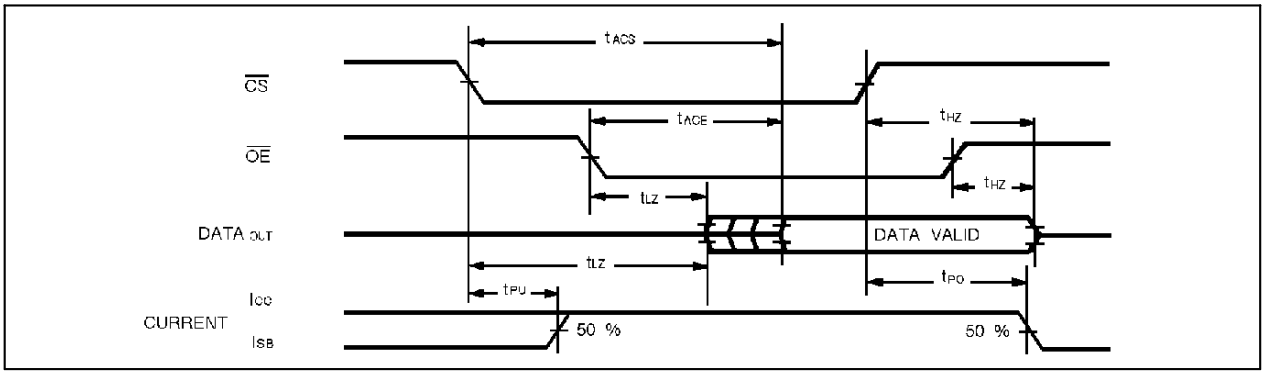
| READ CYCLE | | PARAMETER | L67132–45 L67142–45 | | L67132–55 L67142–55 | | L67132–70 L67142–70 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL (19) | SYMBOL (20) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| | | | PRELIMINARY | | | | | | |
| TAVAVR | $t_{RC}$ | Read cycle time | 45 | – | 55 | – | 70 | – | ns |
| TAVQV | $t_{AA}$ | Address access time | – | 45 | – | 55 | – | 70 | ns |
| TELQV | $t_{ACS}$ | Chip Select access time (18) | – | 45 | – | 55 | – | 70 | ns |
| TGLQV | $t_{AOE}$ | Output enable access time | – | 30 | – | 35 | – | 40 | ns |
| TAVQX | $t_{OH}$ | Output hold from address change | 0 | – | 0 | – | 0 | – | ns |
| TELQZ | $t_{LZ}$ | Output low Z time (16, 17) | 5 | – | 5 | – | 5 | – | ns |
| TEHQZ | $t_{HZ}$ | Output high Z time (16, 17) | – | 20 | – | 30 | – | 35 | ns |
| TPU | $t_{PU}$ | Chip Select to power up time (17) | 0 | – | 0 | – | 0 | – | ns |
| TPD | $t_{PD}$ | Chip disable to power down time (17) | – | 50 | – | 50 | – | 50 | ns |

**Notes :**
16. Transition is measured ± 500 mV from low or high impedance voltage with load (figures 1 and 2).
17. This parameter is guaranteed but not tested.
18. To access RAM $\overline{CS}$ = VIL.
19. STD symbol.
20. ALT symbol.

## Timing Waveform of Read Cycle nº 1, Either Side (21, 22, 24)




## Timing Waveform of Read Cycle nº 2, Either Side (21, 23, 25)



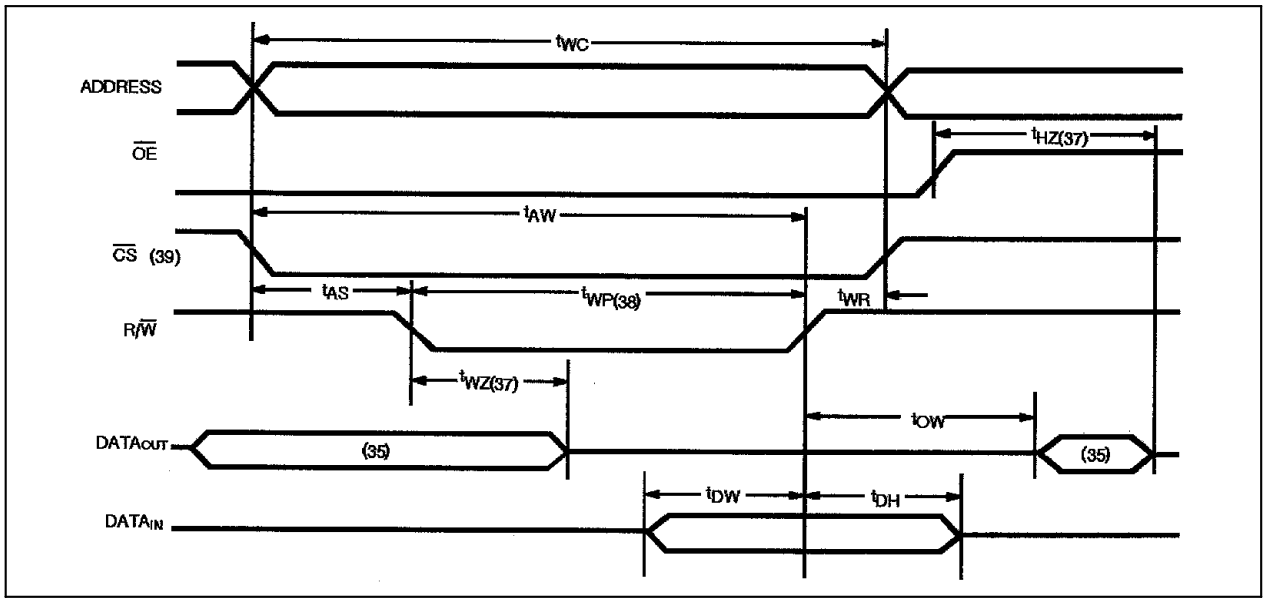

**Notes :**
21. R/$\overline{W}$ is high for read cycles.
22. Device is continuously enabled, $\overline{CS}$ = VIL.
23. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
24. $\overline{OE}$ = $V_{IL}$.
25. To access RAM, $\overline{CS}$ = $V_{IL}$.

## AC Parameters

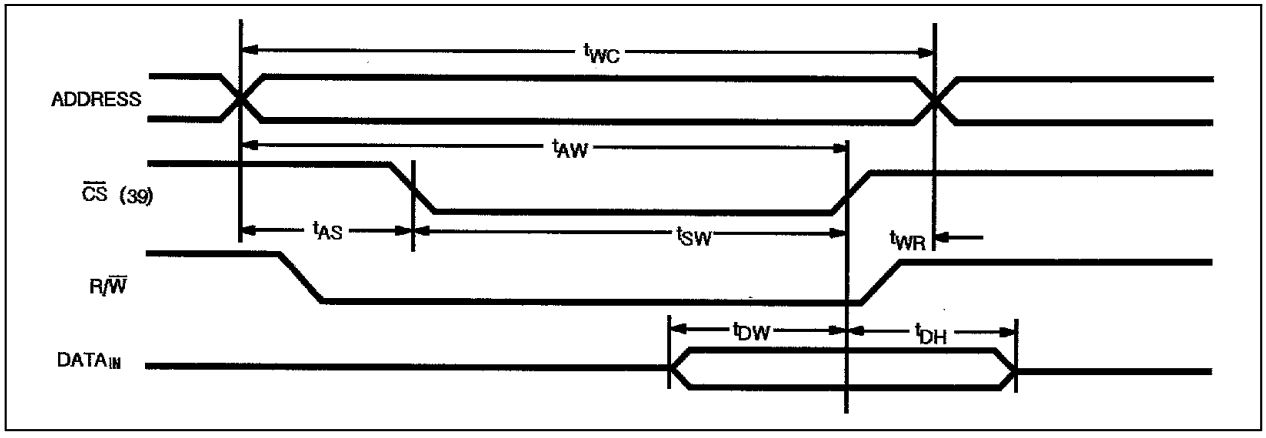
| WRITE CYCLE | | PARAMETER | L67132–45 L67142–45 | | L67132–55 L67142–55 | | L67132–70 L67142–70 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| SYMBOL (30) | SYMBOL (31) | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| | | | PRELIMINARY | | | | | | |
| TAVAVW | $t_{WC}$ | Write cycle time | 45 | – | 55 | – | 70 | – | ns |
| TELWH | $t_{SW}$ | Chip select to end of write (28) | 35 | – | 40 | – | 45 | – | ns |
| TAVWH | $t_{AW}$ | Address valid to end of write | 35 | – | 40 | – | 45 | – | ns |
| TAVWL | $t_{AS}$ | Address Set–up Time | 0 | – | 0 | – | 0 | – | ns |
| TWLWH | $t_{WP}$ | Write Pulse Width | 35 | – | 40 | – | 45 | – | ns |
| TWHAX | $t_{WR}$ | Write Recovery Time | 0 | – | 0 | – | 0 | – | ns |
| TDVWH | $t_{DW}$ | Data Valid to end of write | 25 | – | 25 | – | 30 | – | ns |
| TGHQZ | $t_{HZ}$ | Output high Z time (26, 27) | – | 20 | – | 30 | – | 40 | ns |
| TWHDX | $t_{DH}$ | Data hold time (29) | 0 | – | 0 | – | 0 | – | ns |
| TWLQZ | $t_{WZ}$ | Write enable to output in high Z (26, 27) | – | 20 | – | 30 | – | 40 | ns |
| TWHQX | $t_{OW}$ | Output active from end of write (26, 27, 29) | 0 | – | 0 | – | 0 | – | ns |

**Notes :**
26. Transition is measured ± 500 mV from low or high impedance voltage with load (figures 1 and 2).
27. This parameter is guaranteed but not tested.
28. To access RAM $\overline{CS}$ = VIL.
    This condition must be valid for entire $t_{SW}$ time.
29. The specification for $t_{DH}$ must be met by the device supplying write data to the RAM under all operating conditions.
    Although $t_{DH}$ and $t_{OW}$ values vary over voltage and temperature, the actual $t_{DH}$ will always be smaller than the actual $t_{OW}$.
30. STD symbol.
31. ALT symbol.

## Timing Waveform of Write Cycle nº 1, R/$\overline{W}$ Controlled Timing (32, 33, 34, 38)




## Timing Waveform of Write Cycle nº 2, $\overline{CS}$ Controlled Timing (32, 33, 34, 36)




**Notes :**

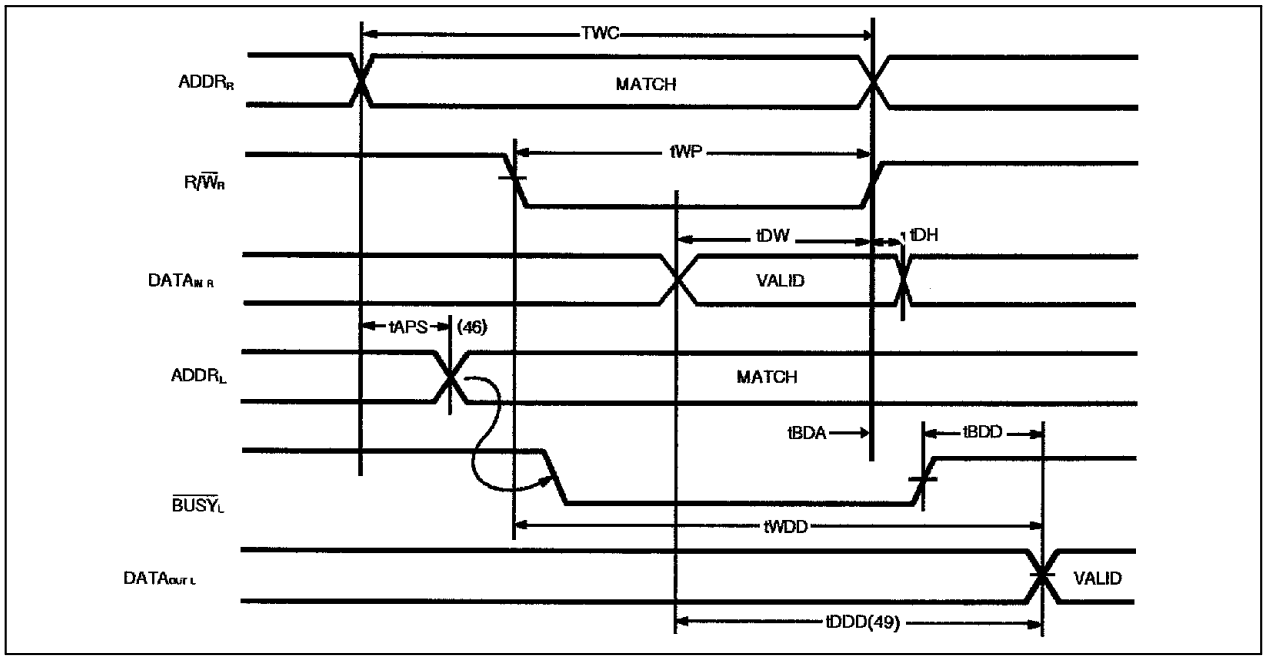
32. R/$\overline{W}$ must be high during all address transitions.
33. A write occurs during the overlap ($t_{SW}$ or $t_{WP}$) of a low $\overline{CS}$ and a low R/$\overline{W}$.
34. $t_{WR}$ is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ going high to the end of write cycle.
35. During this period, the I/O pins are in the output state, and input signals must not be applied.
36. If the $\overline{CS}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
37. Transition is measured ± 500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100 % tested.
38. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($t_{WZ}$ + $t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required $t_{DW}$. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.
39. To access RAM, $\overline{CS}$ = VIL.

## AC Parameters

| SYMBOL | PARAMETER | L67132–45 L67142–45 | | L67132–55 L67142–55 | | L67132–70 L67142–70 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| **BUSY TIMING (For L 67132 only)** | | | | | | | | |
| $t_{BAA}$ | $\overline{BUSY}$ Access time to address | – | 35 | – | 45 | – | 50 | ns |
| $t_{BDA}$ | $\overline{BUSY}$ Disable time to address | – | 35 | – | 40 | – | 40 | ns |
| $t_{BAC}$ | $\overline{BUSY}$ Access time to Chip Select | – | 30 | – | 35 | – | 50 | ns |
| $t_{BDC}$ | $\overline{BUSY}$ Disable time to Chip Select | – | 25 | – | 30 | – | 40 | ns |
| $t_{WDD}$ | Write Pulse to data delay (40) | – | 70 | – | 80 | – | 90 | ns |
| $t_{DDD}$ | Write data valid to read data delay (40) | – | 45 | – | 55 | – | 70 | ns |
| $t_{APS}$ | Arbitration priority set–up time (41) | 5 | – | 5 | – | 5 | – | ns |
| $t_{BDD}$ | $\overline{BUSY}$ disable to valid data | – | Note 42 | – | Note 42 | – | Note 42 | ns |
| **BUSY TIMING (For L 67142 only)** | | | | | | | | |
| $t_{WB}$ | Write to $\overline{BUSY}$ input (43) | 0 | – | 0 | – | 0 | – | ns |
| $t_{WH}$ | Write hold after $\overline{BUSY}$ (44) | 20 | – | 30 | – | 30 | – | ns |
| $t_{WDD}$ | Write pulse to data delay (45) | – | 70 | – | 80 | – | 90 | ns |
| $t_{DDD}$ | Write data valid to read data delay (45) | – | 45 | – | 55 | – | 70 | ns |

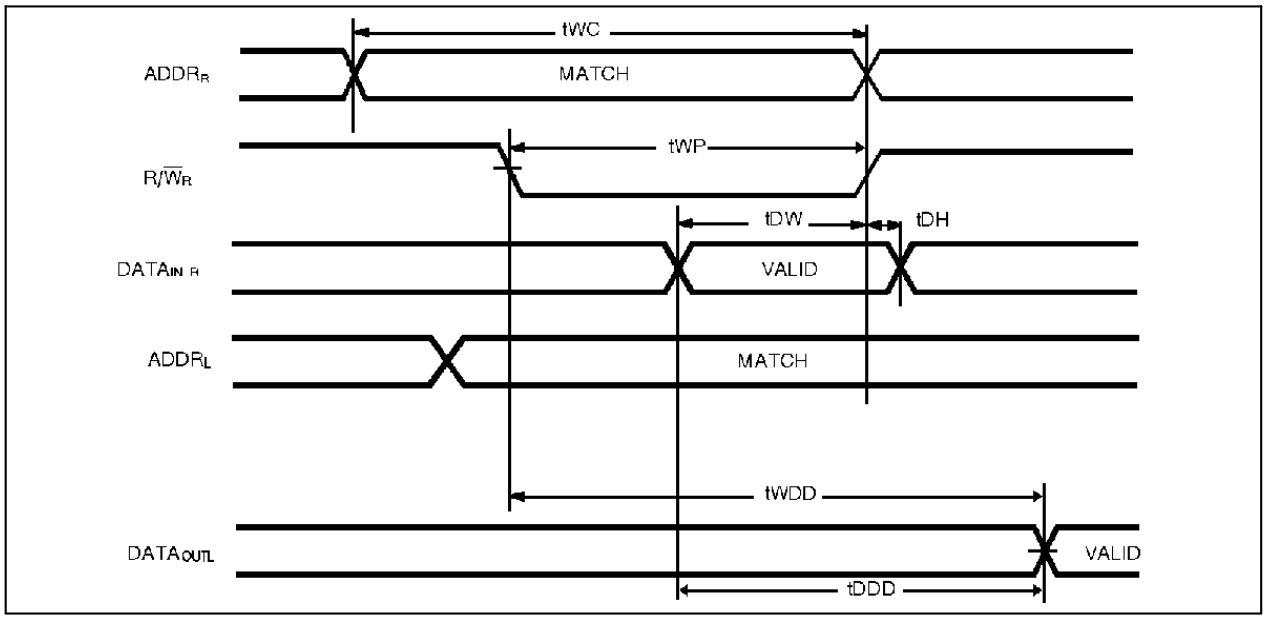
**Notes :**
40. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveform of Read with $\overline{BUSY}$ (For L67132 only)”.
41. To ensure that the earlier of the two ports wins.
42. $t_{BDD}$ is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
43. To ensure that the write cycle is inhibited during contention.
44. To ensure that a write cycle is completed after contention.
45. Port-to-port delay through RAM cells from writing port to reading port, refer to “Timing Waveforms of Read with Port to port delay (For L67142 only)”.

## Timing Waveform of Read with $\overline{BUSY}$ (46, 47, 48) (For L 67132)



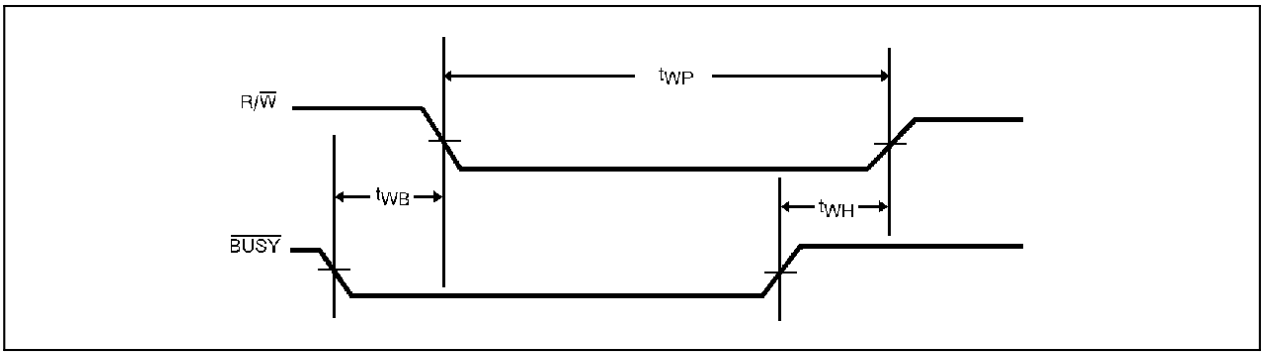

**Notes :**
46. To ensure that the earlier of the two port wins.
47. Write cycle parameters should be adhered to, to ensure proper writing.
48. Device is continuously enabled for both ports.
49. $\overline{OE}$ at L for the reading port.

## Timing Waveform of Write with Port-to-port (50, 51, 52) (For L 67142 only)

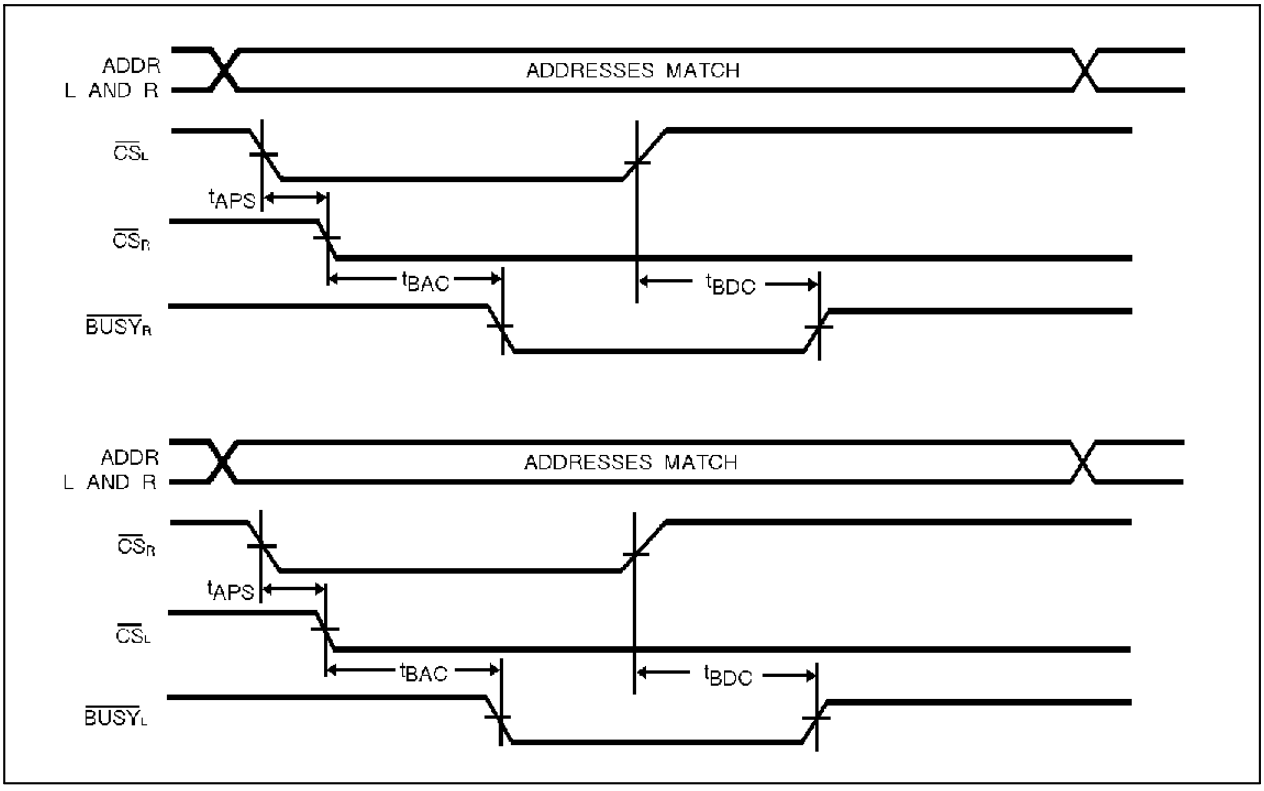



**Notes :**
50. Assume $\overline{BUSY}$ = H for the writing port, and $\overline{OE}$ = L for the reading port.
51. Write cycle parameters should be adhered to, to ensure proper writing.
52. Device is continuously enabled for both ports.

### Timing Waveform of Write with $\overline{BUSY}$ (For L 67132)

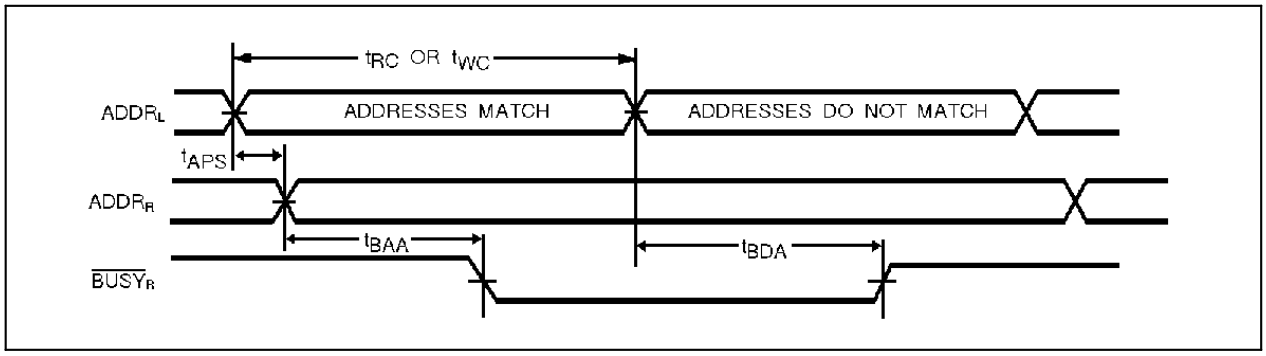



### Timing Waveform of Contention Cycle nº 1, $\overline{CS}$ Arbitration (For L 67132 only)

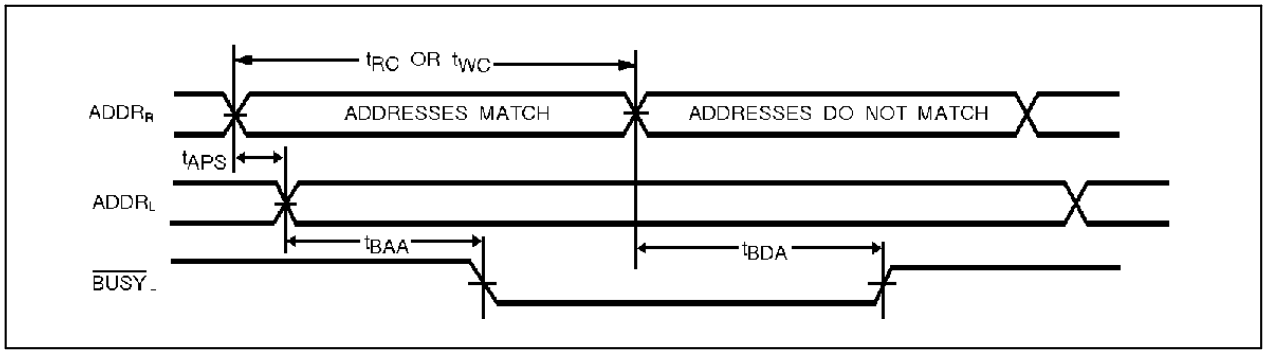


### Timing Waveform of Contention Cycle nº 2, Address Valid Abritration (For L 67132 only) (53)

Left Address Valid First :

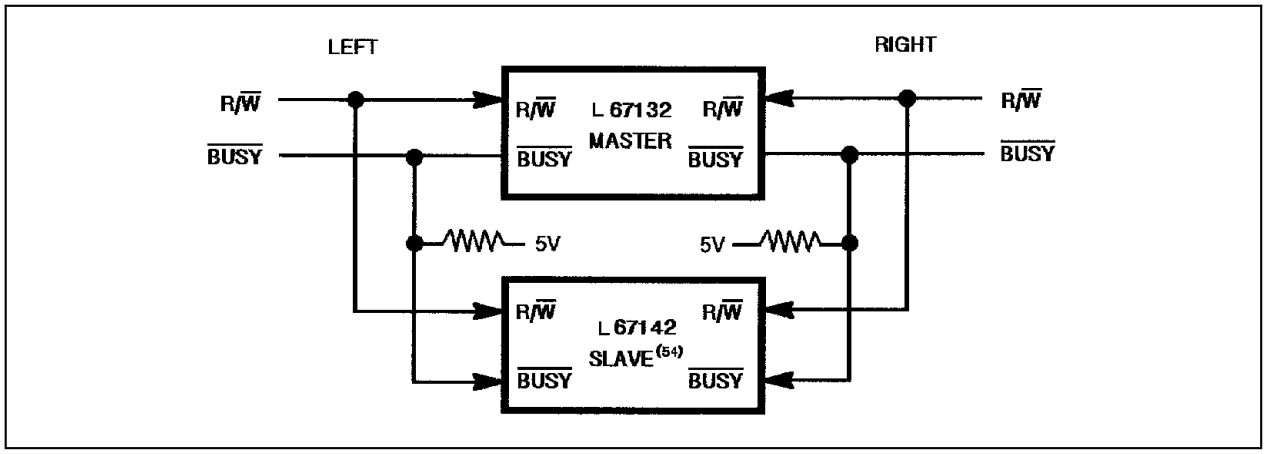



Right Address Valid First :




**Note :** 53. $\overline{CS}_L = \overline{CS}_R = V_{IL}$

### 16 Bit Master/Slave Dual-port Memory Systems




**Note :** 54. No arbitration in L 67142 (SLAVE). $\overline{BUSY}$-IN inhibits write in L 67142 (SLAVE).

## Ordering Information

TEMPERATURE RANGE PACKAGE DEVICE SPEED FLOW

**C** **L** **S3** — **67132V** — **55**

3.3 V ± 0.3 Volt

1K = 48 pin DIL ceramic 600 mils
CK = 48 pin DIL side-brazed 600 mils
4K = 48 pin LCC
S3 = 52 pin PLCC
3K = 48 pin DIL plastic 600 mils
RD = 64 pin VQFP

45 ns
55 ns
70 ns

blank = MHS standards
/883 = MIL-STD 883 Class B or S
P883 = MIL-STD 883 + PIND TEST
SB/SC = SCC 9000 level B/C
SHXXX = Special customer request
FHXXX = Flight models (space)
MHXXX = Mechanical parts (space)
LHXXX = Life test parts (space)

67132 = 16K (2K × 8) Master
67142 = 16K (2K × 8) Slave
L = Low power
V = Very low power
EL = Low power and rad tolerant
EV = Very low power and rad tolerant

C = Commercial 0° to +70°C
I = Industrial –40° to +85°C
A = Automotive –40° to +125°C
M = Military –55° to +125°C
S = Space –55° to +125°C